32.5 A 6.25GHz 1V LC-PLL in 0.13µm CMOS

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A 6.25GHz PLL with integrated LC-tank VCO and on-chip loop filter (LF) was designed and fabricated in 0.13µm CMOS technology. Operated at 1V with an input reference clock at 62.5MHz, the output clock jitter is $0.5ps_{rms}$. This PLL is designed for 6.25 to 12.5Gb/s serial backplane communication systems where quadrature clocks for data/clock recovery are desired [1, 2].

The PLL includes a phase-frequency detector (PFD), a leakage-canceling charge pump (CP), an integrated LF, a low-noise LC VCO and a high-speed divider. The use of a phase-interpolater-based clock and data recovery approach necessitates quadrature 6.25GHz clocks for 12.5Gb/s operation. These can be produced either by a single 12.5GHz VCO driving subsequent divide-by-2 circuits or by coupled 6.25GHz VCOs oscillating in quadrature. The 12.5GHz VCO solution is problematic since parasitics make it difficult to realize an inductor with high enough Q and self-resonant frequency. Thus, quadrature (I/Q) outputs are realized by cross coupling two LC-VCO tanks operating at 6.25GHz as shown in Figure 32.5.1 [3]. An N-poly over N-well capacitor is selected as a varactor and is carefully designed to have sufficiently high Q and a large Cmax/Cmin ratio of about 2.5. A 1.1GHz tuning range is achieved around a 6.25GHz center frequency with the aid of a CP having near rail-to-rail operation. An inductor with a Q of 20 is implemented by using the top four layers in a 7-metal-layer process to reduce coupling to the substrate. To circumvent the low (2Ωcm) resistivity of the substrate, a patterned ground shield is used to combat substrate losses. Analog tuning via the varactors is used to avoid the Q degradation often associated with digitally switched capacitor banks. Both cross-coupled PMOS and NMOS transistors are used in the VCO topology to prevent excursions above the positive supply rail, which might reduce reliability. The layouts of the two VCOs are carefully matched to avoid oscillation-frequency offset, which would degrade phase noise performance.

Selection of the proper LF BW and damping factor is critical for optimum jitter generation and transfer. The loop BW must be set high enough to suppress close-in VCO phase noise and low enough to reject unwanted jitter in the reference clock source. The PLL is designed to operate with a reference clock frequency ranging from 62.5 to 312.5MHz. A programmable CP and LF set the PLL BW to 3% of the reference clock frequency to improve overall jitter performance by providing a near optimal trade off of reference clock noise and intrinsic VCO noise. The damping factor is set to 3 to minimize jitter peaking and maximize loop stability. Since MOS capacitors exhibit large variations over the PLL operating range, linear MIM capacitors are used in the LF. The dividers are implemented using CML circuits to minimize jitter and supply noise injection while achieving 8GHz operation across all PVT corners.

To maintain a reasonable tuning range at low supply voltages, it is critical to maximize the CP output range. Conventional CP designs suffer from headroom limitations that cause the CP current to diminish when the output comes within V_{DS_sat} of either rail. For example, a typical CP maintains full output current over only 50% of its operating range when V_{DD} = 1V and V_{DS_sat} = 0.25V (see Fig. 32.5.2). This variation of CP current causes loop dynamics to vary with different output frequencies and PVT corners. These issues are avoided by a CP design that outputs constant current even when its output voltage is very close to the rails. Figure 32.5.3 shows the top half of the CP circuit, which produces constant current for outputs close to the supply voltage. It consists of a CP driver along with its replica and a CP output circuit along with its replica. Low swing CML logic is used to minimize spurious tones from the reference clock. $N1$ provides a constant reference current to the CP output replica. When CP_OUT goes high, the opamp forces VCP0 to go down and VCP1 to go up, forces the switching node VCP2 to go down and generates a pulse to overdrive P2 and maintain constant output current. This approach allows the CP to achieve constant current when CP_OUT is only 5mV below V_{DD}. This increases the VCO control voltage range by 2× relative to traditional CP designs.

Ultra-low CP leakage current is also critical for low-jitter operation. With the scaling of CMOS technology, leakage current can become severe, especially at high temperatures and process corners. In traditional CP designs the leakage current could be as high as 5% of the operating current in a 0.13µm process. For a 62.5MHz reference clock and a divider ratio of 100, the integration of this leakage current over 100 VCO periods could generate as much as$10ps_{rms}$ jitter on the output. The noise on the control voltage severely degrades the PLL operation. CMOS transistors operating in weak inversion have a leakage current $I_s = I_o \exp((V_{gs} - V_t)/nV_t)(1 - \exp(-V_{ds}/V_t))$, where I_o is process and temperature dependent. The leakage current is not only dependent on process and temperature, but also on the operating voltage (V_{ds}) [4]. This means that the CP output voltage strongly influences the leakage current. The difference between the leakage currents of the PMOS and NMOS devices in the CP is integrated by the LF. This design cancels the net leakage current from the supply rail using the circuit shown in Fig. 32.5.4. N1 and P1 model the leakage currents of the CP when it is off. The opamp feedback loop forces N2 to generate the current required to reproduce the CP output voltage in the replica circuit. N3, which is a copy of N2, is then used to cancel the leakage current from P2. The circuit is designed to handle leakage currents ranging from 1nA to 10µA with sufficient accuracy, supply noise rejection, and stability. The circuit cancels 99% of the leakage current across all PVT and PLL operating corners.

Figure 32.5.5 shows a micrograph of the LC-PLL integrated in a 6.25 to 12.5Gb/s serial backplane communication chip. The chip was fabricated in a 0.13µm CMOS technology with seven levels of metal and assembled in a 361-pin organic flip-chip BGA package. The PLL occupies $0.43mm^2$ and consumes 25mW of power. Figure 32.5.6 shows the measured output spectrum of the PLL. The PLL output jitter is $0.57ps_{rms}$ integrated over a 1kHz to 1GHz band. A 62.5MHz input reference clock with a jitter of $2.5ps_{rms}$ over the same band is used for the measurement. Excluding the tester's noise floor of $0.25ps_{rms}$, the PLL jitter is $0.5ps_{rms}$. The 62.5MHz reference clock tone is -115dBc due to the use of a low-swing CML-type CP. Figure 32.5.7 shows an eye diagram of a 6.25Gb/s transmitter [1] clocked by this PLL for a $2^{31} - 1$ PRBS data pattern with $16ps_{pp}$ jitter.

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References:
[1] P. Landman et al., "A Transmit Architecture with 4-Tap Feed Forward Equalization for 6.25/12.5 Gbs/Serial Backplane communications,"*IEEE ISSCC Dig. Tech. Papers*, pp.66-67, Feb., 2005.
[2] B. Payne et al., "A 6.25Gb/s Binary Adaptive DFE with First Post-Cursor Tap Cancellation for Serial Backplane Communications," *IEEE ISSCC Dig. Tech. Papers*, pp.68-69, Feb., 2005.
[3] T.P. Liu, "1.5 V 10-12.5 GHz Integrated CMOS Oscillators," *Symp. on VLSI Circuits*, pp55-56, 1999.
[4] R.X. Gu and M.I. Elmasry, "Power Dissipation Analysis and Optimization of Deep submicron CMOS digital Circuits," *IEEE J. Solid-State Circuits*, vol. 31, pp.707-713, May, 1996.

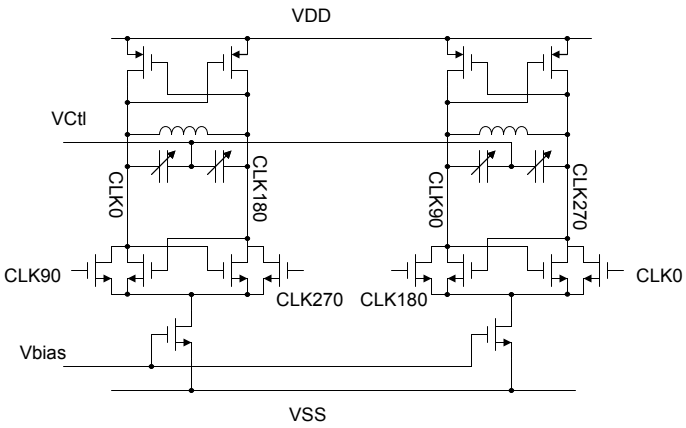

Figure 32.5.1: Cross-coupled 4-phase LC-VCO.

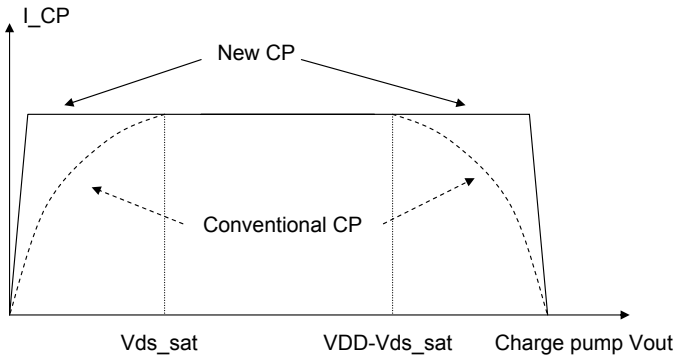

Figure 32.5.2: Comparisons of conventional and rail-rail CP designs.

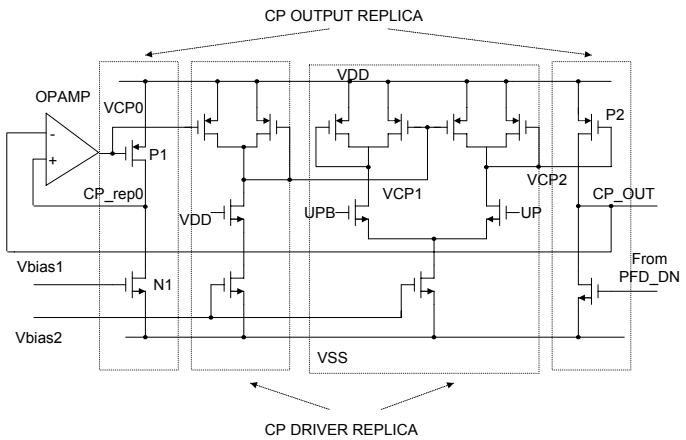

Figure 32.5.3: Schematic of rail-rail CP design.

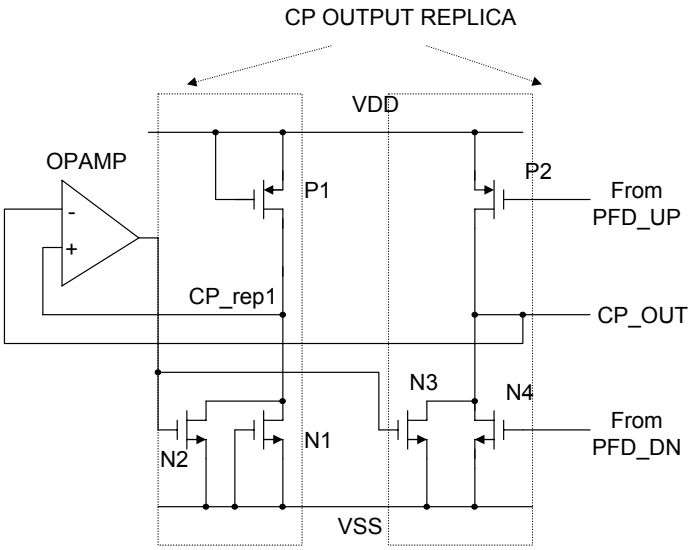

Figure 32.5.4: Schematic of leakage cancellation CP design.

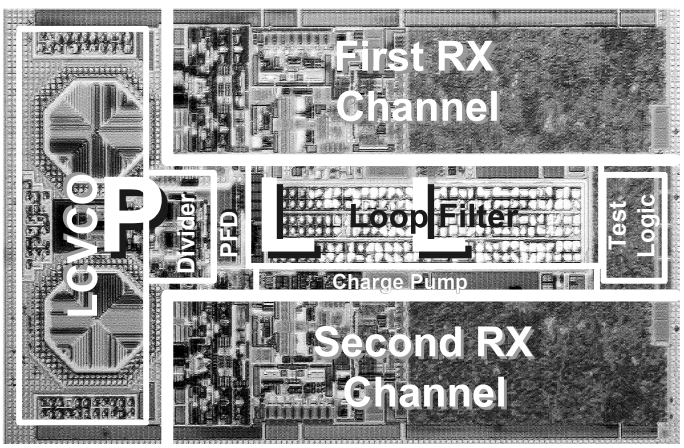

Figure 32.5.5: Die micrograph.

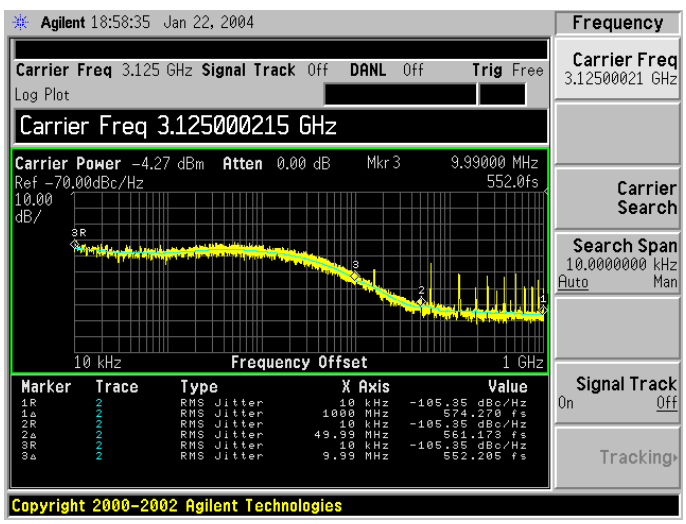

Figure 32.5.6: Measured spectrum of 6.25GHz clock.

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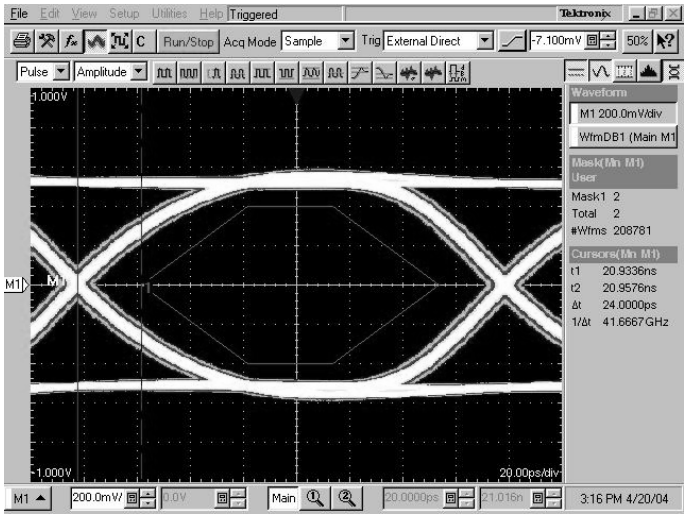

Figure 32.5.7: Measured eye of 6.25GB/s transmitter 2^{31}-1 PRBS.

